Notice of Allowability	Application No.	Applicant(s)	
	10/743,377	KIM ET AL.	
	Examiner	Art Unit	
	Pamela E. Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the application papers filed 23 December 2003*.

2. ☒ The allowed claim(s) is/are *1-8*.

3. ☒ The drawings filed on *23 December 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

DETAILED ACTION

This office action is in response to the filing of the application papers on 23 December 2003. Claims 1-8 are pending.

Allowable Subject Matter

Claims 1-8 are allowed.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance: prior art does not anticipate, teach, or suggest a method of fabricating memory with nano dots where (a) a first insulating layer, a charge storage layer, a sacrificial layer, and a metal layer are sequentially deposited on a substrate in which source and drain electrodes are formed; (b) forming a plurality of holes on the resultant structure by anodizing the metal layer and oxidizing portions of the sacrificial layer that are exposed through the holes; (c) patterning the charge storage layer to have nano dots by removing the oxidized metal layer, and etching the sacrificial layer and the charge storage layer using the oxidized sacrificial layer as a mask; and (d) removing the oxidized sacrificial layer, depositing a second insulating layer and a gate electrode on the patterned charge storage layer, and patterning the first insulating layer, the patterned charge storage layer, the second insulating layer, and the gate electrode to a predetermined shape.

For example, Craighead et al. (6,753,200) disclose a method of fabricating memory with dots where a first insulating layer (42), a charge storage layer (44), a sacrificial layer (46), and a layer (48) are sequentially deposited on a substrate

(40) in which source and drain electrodes are formed; forming a plurality of holes (52) on the resultant structure; (c) patterning the charge storage layer (44) to have dots by removing the layer (48), and etching the sacrificial layer (46) and the charge storage layer (44) using the sacrificial layer (46) as a mask; and removing the sacrificial layer (46) (Fig. 4a; col. 8, line 31 thru col. 9, line 45).

However, Craighead et al. do not disclose, anticipate, teach, or suggest a method of fabricating memory with nano dots where a plurality of holes on the resultant structure are formed by anodizing the metal layer and oxidizing portions of the sacrificial layer that are exposed through the holes; patterning the charge storage layer to have nano dots by removing the oxidized metal layer, and etching the sacrificial layer and the charge storage layer using the oxidized sacrificial layer as a mask; and removing the oxidized sacrificial layer, depositing a second insulating layer and a gate electrode on the patterned charge storage layer, and patterning the first insulating layer, the patterned charge storage layer, the second insulating layer, and the gate electrode to a predetermined shape.

Ugajin et al. (5,608,231) disclose a method of fabricating memory with dots where (a) three layers (2a, 3, 2b) are sequentially deposited on a substrate (1) in which source and drain electrodes are formed (Fig. 9); patterning the layers to have dots (Fig. 10); and depositing a fourth layer (2c) and a gate electrode (G) on the patterned layers (Fig. 11-12; col. 10, lines 13-49). However, Ugajin et al. do not disclose, anticipate, teach or suggest a method of fabricating memory with nano dots where a first insulating layer, a charge storage layer, a sacrificial layer, and a metal layer are sequentially deposited on a substrate in which source and

drain electrodes are formed; forming a plurality of holes on the resultant structure by anodizing the metal layer and oxidizing portions of the sacrificial layer that are exposed through the holes; patterning the charge storage layer to have nano dots by removing the oxidized metal layer, and etching the sacrificial layer and the charge storage layer using the oxidized sacrificial layer as a mask; and removing the oxidized sacrificial layer, depositing a second insulating layer and a gate electrode on the patterned charge storage layer, and patterning the first insulating layer, the patterned charge storage layer, the second insulating layer, and the gate electrode to a predetermined shape.

Kim (6,767,771) discloses a method of fabricating memory with nano dots where a first insulating layer (35), a sacrificial layer (37), and a metal layer (39) are sequentially deposited on a substrate (30) in which source and drain electrodes (31, 33) are formed (Fig. 10A-10C); oxidizing portions of the sacrificial layer (37) (Fig. 10D); patterning the sacrificial layer (37) to have nano dots by removing the oxidized sacrificial layer (Fig. 10E); and depositing a second insulating layer (41) and a gate electrode (43) on the patterned sacrificial layer (37) (Fig. 10F). However, Kim does not disclose, anticipate, teach or suggest sequentially depositing a first insulating layer, a charge storage layer, a sacrificial layer, and a metal layer are sequentially deposited on a substrate; forming a plurality of holes on the resultant structure by anodizing the metal layer and oxidizing portions of the sacrificial layer that are exposed through the holes; patterning the charge storage layer to have nano dots by removing the oxidized metal layer, and etching the sacrificial layer and the charge storage layer using

the oxidized sacrificial layer as a mask; and removing the oxidized sacrificial layer, depositing a second insulating layer and a gate electrode on the patterned charge storage layer, and patterning the first insulating layer, the patterned charge storage layer, the second insulating layer, and the gate electrode to a predetermined shape.

The prior art made of record in this action does not anticipate, teach, or suggest a method of fabricating memory with nano dots where a first insulating layer, a charge storage layer, a sacrificial layer, and a metal layer are sequentially deposited on a substrate in which source and drain electrodes are formed; forming a plurality of holes on the resultant structure by anodizing the metal layer and oxidizing portions of the sacrificial layer that are exposed through the holes; patterning the charge storage layer to have nano dots by removing the oxidized metal layer, and etching the sacrificial layer and the charge storage layer using the oxidized sacrificial layer as a mask; and removing the oxidized sacrificial layer, depositing a second insulating layer and a gate electrode on the patterned charge storage layer, and patterning the first insulating layer, the patterned charge storage layer, the second insulating layer, and the gate electrode to a predetermined shape.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E. Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP

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